

REMARKS

Reconsideration of the subject application is respectfully requested.

Claims 1-20 were rejected as being anticipated by Willis (US 5,329,369) or obvious in view of Willis when combined with secondary references cited by the Examiner. These grounds of rejection are respectfully traversed especially in view of the forgoing amendments to the claims.

The present invention and Willis are directed to two entirely different problems. In the environment of the present invention, typically a camera image is input to a display controller where it is cropped and scaled (resized), and then sent to a display where the image is shown in a sub-window (picture-in-picture or PIP window) of the main display window. The dimensions of the PIP window must match the dimensions of the resized camera image or the image will not display properly. Therefore, whenever the dimensions of the PIP window or the resized camera image are changed by setting internal registers of the controller, the dimension of the PIP window and the resized camera image will not match for the time it takes to write the registers. This temporary size mismatch will create corruption or “tearing” of the camera image on the display until the camera image and the PIP window size are equal.

The present invention overcomes this problem by synchronizing the change in dimension values in the registers of the controller that specify the resized camera image and the PIP window. Specifically, the present invention (Claim 1) provides a completion signal indicating completion of changing the first set of dimension values and the second set of dimension values; receiving a trigger signal indicating a beginning of a new image to be displayed; and implementing the changed first set of dimension values and the changed second set of dimension values upon receiving the trigger signal while the completion signal is being provided. Claim 15 recites image synchronization circuitry configured to recognize an asserted enable bit setting in any dimension register of the first set of dimension registers and the second set of dimension registers, the image synchronization circuitry being further configured to implement dimension values stored in each of the first set of dimension registers and the second set of dimension registers upon both recognizing the asserted enable bit setting and receiving a trigger signal

indicating a beginning of a new image to be displayed. The remaining dependent claims recite additional features directed to the specific solution of the present invention.

Willis is not remotely concerned with the problem addressed by the present invention and clearly does not disclose or suggest the specific solution recited in the claims. Willis is directed to a very specific problem: if an auxiliary picture developed by a picture-in-picture processor from an auxiliary source were displayed on a wide screen television, the picture would be geometrically distorted or would not fill the screen (col. 2, line 62 – col. 3, line 7). Willis solves this problem by providing a signal processor for distorting a video signal such that on subsequent display the picture will exhibit no aspect ratio distortion. The distortion is generally implemented as asymmetric compression (col. 3, lines 8-17).

In rejecting the claims the Examiner very generally points to parts of the Willis patent but such areas all relate to details of the asymmetric compression as implemented in the Willis invention. They have nothing at all to do with synchronizing the change in dimension values in registers in a display controller, where the dimensions specify a display region in which a resized camera image is displayed and a picture-in-picture window. The Examiner points to column 21, lines 23-35 of Willis for a discussion of synchronization but this relates to synchronizing two different video sources – auxiliary video data and main video data, which clearly has nothing to do with the presently claimed invention. The secondary references cited by the Examiner are similarly irrelevant to the present invention and fail to supply the features that are missing from Willis.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration of the present application.

Respectfully submitted,

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